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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,396	02/21/2002	Tadaaki Maeda	03500.016212.	5609

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EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,396	MAEDA, TADAAKI	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02212002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "11" and "31" have both been used to designate "A Memory Controller" and reference characters "13" and 33" have both been used to designate "A Power Controller". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: Spelling "Date" should be "Data" page2 of Detailed Description paragraph 2.

3. The disclosure is objected to because of the following informalities: Spelling "PreChange" should be "PreCharge" on page 2 paragraph 5 [0021].

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kakimi (U.S. Patent No. 5,640,357)

Kakimi teaches the invention comprising:

A memory controller [52] for outputting a clock enables signal [RAS E9, CAS E10, fig.3]; a power controller [54, 70, fig. 3];

Pull-down resistance [66, 68, fig. 3]; and wherein

upon detection of power stoppage of the main power supply [col. 11 lines 54-58, col. 12 lines 63-67], the power controller switches the DRAM power supply to the battery power supply [col. 12, line 67 – col. 13, line 1]; and

the memory controller changes the clock enable signal for the DRAM to the low level to establish the self-refresh mode based upon the power stoppage signal [reset signal E5, col. 11, lines 60-61] from the power controller whereby the low level signal is being maintain by the pull-down resistance for maintaining the self-refresh mode [col. 11, line 60 – 12, line 8, col. 14, lines 29-41] while the power supply thereto is stopped [col. 14, lines 43-47].

5. As per claim 5, Kakimi teaches wherein power is supplied to memory controller only by main power [fig. 3], and, if main power is stopped, the power is supply to memory controlled until the self-refresh mode of DRAM is established [col. 9 lines 17-51].

6. As per claim 6, George teaches wherein, if power controller detects stoppage of main power, power controller instructs the self-fresh mode by changing an instruction signal for instructing the self-refresh mode to memory controller to active [col. 3 lines 67 to col. 4 lines 1-2].

7. As per claim 7, Kakimi teaches wherein, if power controller detects stoppage of main power, power controller maintains an instruction signal for self-refresh mode [fig. 6A - "backup inst. Signal"] to active until main power restore and after the instruction signal was made active, system reset is cancel [col. 11 lines 23-35]; and

while the instruction signal is active, the memory controller maintains the clock enable signal [E6, E7, fig. 9] to low level [col. 11 lines 28-32].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negative by the manner in which the invention was made.

9. Claims 1-4, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over George (U.S. Patent No. 6,317,657) in view of Kakimi (U.S. Patent No. 5,640,357)

10. George teaches a memory device substantially as claimed comprising:

A memory control device [SRCM] for outputting a clock enable signal [col. 3 lines 11-14].

A power controller [fig. 1 – "BBM"] for detecting power stoppage of said main power supply [col. 3 lines 14-17]; and switching power supply for DRAM from main to battery [col. 3 lines 20-23]; and

Instructs a self-refresh mode to memory controller [col. 3 line 67 to col. 4 lines 1-2]; memory controller changes the clock enable signal for DRAM to low level to establish the self-refresh mode of DRAM [col. 4 lines 6-11].

However, George does not teach wherein after DRAM is set to the self-refresh mode, the supplying of power to memory controller is stopped, and even after the stoppage, the clock enable signal is maintained to low level by pull-down resistance.

Kakimi teaches, after DRAM is set to self-refresh mode, the supplying of power to said memory controller is stopped [col. 4 lines 48-54]; and

After the stoppage, the clock enable signal is maintained to the low level by pull down- resistance [col. 12 lines 2-8].

Thus, it would have been obvious to one skilled in the art at the time to combine teachings of George and Kakimi to prevent loss data in memory during emergency power failures and, further, to reduce power consumption in battery back up.

11. As per claim 2, George teaches wherein, if power controller detects the power stoppage of main power, power controller switching a power supply for memory [col. 3 lines 16-26]

George does not teach, after self-refresh mode of DRAM is established, batter power supply to memory controller is stop. However, Kakimi teaches wherein only

backup power is supplied to the RAM [col. 4 lines 49-50]. Thus, it would have been obvious to one skilled in the art at the time to apply Kakimi's teaching for the reasons discuss above in claim 1.

12. As per claim 3, Kakimi teaches, when the main power source is shut off, backup power is supplied only to the DRAM [col. 4 lines 48-50]

13. As per claim 4, Kakimi teaches, after DRAM established self-refresh, power supply controller stops supplying power to memory controller [col. 11 lines 42-53 – "power line 74" see fig. 3].

14. As per claim 10, George teaches wherein power controller monitors voltage of main power [col. 3 lines 14-18].

15. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over George/Kakimi as applied to claim 1 above, and further in view of Baweja (U.S. Patent No. 6,212,599)

16. As per claim 8, George/Kakimi does not teach wherein, when main power is normally being on, memory controller executes power-on initial; but when main power is restored, after the power stoppage, the memory controller does not execute the power-on initial sequence for DRAM. However, Baweja teaches wherein, upon power on, SDRAM is initialized [col. 7 lines21-27]; and, upon waking up from main power stoppage, SDRAM initialization is avoided [col. 7 lines 55-61]. At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Baweja's method to George/Kakimi's memory control device, in order to maintain the data in the memory [col. 7 lines 62].

17. As per claim 9, George/Kakimi teaches wherein power controller makes an instruction signal for the self-refresh mode inactive when main power is normally being ON [fig. 9C "Backup instruction signal"] and maintains the instruction signal to active until immediately after the system reset is cancelled [col. 12 lines 19-43]. However, George/Kakimi is silent wherein memory controller determines whether or not the power-on initial sequence for DRAM in accordance with the fact whether the instruction signal is active or not. Baweja teaches if "SUS_STAT" is active, DRAM enter normal operation mode without initializing [fig. 5].

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Abe (U.S. Patent No. 5,590,082)

Dias (U.S. Patent No. 4,977,537)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran

THOMAS LEE
PATENT EXAMINER
TECHNOLOGY CENTER 2100